WEEKLY REPORT

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| Project: | New FPGA trace analyzer |
| Team member: | He Dai, Zhenning Jiang, Hui Li |
| Week ending: | Oct 24, 2014 |

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| He Dai |
| **Completed Deliverables:**   * Vivado Tutorial: Zynq tutorial * Linux installed(Ubuntu) * All Programmable SoC Hardware * PPT prepared   **Time Spend:** 3 hours every day, totally 21 hours  **Difficulties Encountered:**   * Software installed(like Vivado, reinstalled for lots of time)   **Activities to be started next week:**   * Trace Core Design with sample designs |

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| Zhenning Jiang |
| **Completed Deliverables:**   * All Programmable SoC software (8 hours) * PPT prepared(communicate with teammates about what I have learned) (8 hours)   **Time Spend:** 16 hours  **Difficulties Encountered:**   * Software installed(like Vivado, reinstalled for lots of time)   **Activities to be started next week:**   * Block RAM IP Design and Driver IP Design |

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| Hui Li |
| **Completed Deliverables:**   * LabVIEW tutorial (6 hours) * Knowledge reviewing and PPT prepared(communicate with teammates about what I have learned) (4 hours) * Familiar study of LabVIEW tool(Find more examples about LabVIEW and have a further study) (3 hours) * Weekly report(Get information from others and manage a report) (1 hour)   **Time Spend:** 14 hours  **Activities to be started next week:**   * LabVIEW-GUI Prototype Design |